CLAIMS

Subt A'

1. An electronic component comprising:

a substrate; and

an airbridge located over the substrate and having at least a first layer and a second layer over the first layer,

wherein:

the airbridge is electrically conductive; and

the first layer of the airbridge is less resistive than the second layer of the airbridge.

2. The electronic component of claim 1 wherein:

the second layer is a passivation layer.

3. The electronic component of claim 1 wherein:

the second layer is harder than the first layer.

4. The electronic component of claim 1 wherein:

a gap exists between a portion of the airbridge and the substrate; and

a thickness of the second layer is less than a combined thickness of the first layer and the gap.

5. The electronic component of claim 4 wherein:

the thickness of the second layer is less than fifty percent of the combined thickness of the first layer and the gap.

6. The electronic component of claim 1 wherein:

the second layer is located underneath an edge of the first layer.

7. The electronic component of claim 1 wherein:

the second layer is absent underneath a center portion of a width of the airbridge.

8. The electronic component of claim 1 wherein:

a gap exists underneath a portion of the airbridge; and

the gap is unsealed underneath the portion of the airbridge.

9. The electronic component of claim 1 wherein:

the second layer of the airbridge has a compressive stress level of approximately 0 to 200 MegaPascals.

10. The electronic component of claim 1 wherein:

the airbridge further comprises:

a third layer underneath the first layer; and

the third layer is more resistive than the first layer.

11. The electronic component of claim 10 wherein:

the second layer is more resistive than the third layer.

12. The electronic component of claim 1 wherein:

the second layer of the airbridge is electrically conductive.

13. The electronic component of claim 1 wherein:

the second layer of the airbridge is electrically insulative.

Subt a3

14. A semiconductor component comprising:

a semiconductor substrate;

a semiconductor device supported by the semiconductor substrate;

a first electrically insulative layer overlying the semiconductor substrate and the semiconductor device; and

an airbridge located over the semiconductor substrate, located over the first electrically insulative layer, and electrically coupled to the semiconductor device,

wherein:

the airbridge has a first electrically conductive layer; and

the airbridge has a second electrically insulative layer overlying the first electrically conductive layer.

Subt a4

15. The semiconductor component of claim 14 wherein:

a gap exists between a portion of the airbridge and the first electrically insulative layer;

the second electrically insulative layer is a passivation layer harder than the first electrically conductive layer; and

the airbridge further comprises:

an electrically conductive barrier layer located underneath the first electrically conductive layer and more resistive than the first electrically conductive layer.

16. The semiconductor component of claim 15 wherein:

a thickness of the second electrically insulative layer is less than fifty percent of a combined thickness of the electrically conductive barrier layer, the first electrically conductive layer, and the gap.

17. The semiconductor component of claim 15 wherein:

the second electrically insulative layer is devoid of sealing the gap underneath the portion of the airbridge.

18. The semiconductor component of claim 14 wherein:

the second electrically insulative layer is absent underneath a center portion of a width of the airbridge.

19. The semiconductor component of claim 14 wherein:

the second electrically insulative layer has a compressive stress level of approximately 100 MegaPascals.

20. A method of manufacturing an electronic component comprising:

providing a substrate;

forming a first layer over the substrate to form a first portion of an airbridge; and

forming a second layer over the first layer to form a second portion of the airbridge over the substrate,

wherein:

the airbridge is electrically conductive; and

the first layer of the airbridge is less resistive than the second layer of the airbridge.

21. The method of claim 20 further comprising:

forming a semiconductor device at least partially located within the substrate; and

forming an electrically insulative layer over the substrate and the semiconductor device,

wherein:

forming the first layer further comprises:

providing the first layer comprised of an electrically conductive material; and

forming the second layer further comprises:

providing the second layer comprised of an electrically insulative material.

22. The method of claim 20 further comprising:

forming a semiconductor device at least partially located within the substrate;

forming an electrically insulative layer over the substrate and the semiconductor device; and

forming a sacrificial layer over a portion of the substrate before forming the first layer comprising:

reflowing the sacrificial layer; and

baking the sacrificial layer.

23. The method of claim 22 wherein:

forming the sacrificial layer further comprises:

providing photoresist for the sacrificial layer; and

developing the sacrificial layer before reflowing the sacrificial layer.

24. The method of claim 23 wherein:

forming the sacrificial layer further comprises:

avoiding exposing the sacrificial layer to deep ultra violet light after developing the sacrificial layer.

25. The method of claim 22 wherein:

reflowing the sacrificial layer further comprises:

ramping a reflow temperature from a first temperature up to a second temperature during a first period of time;

heating the sacrificial layer from the first temperature up to the second temperature during the first period of time; and

heating the sacrificial layer at the second temperature during a second period of time; and

baking the sacrificial layer further comprises:

ramping a baking temperature from a third temperature up to a fourth temperature during a third period of time;

heating the sacrificial layer from the third temperature up to the fourth temperature during the third period of time; and

heating the sacrificial layer at the fourth temperature during a fourth period of time.

26. The method of claim 25 wherein:

baking the sacrificial layer further comprises:

providing the third temperature equal to the second temperature.

27. The method of claim 22 further comprising:

removing the sacrificial layer after forming the first layer.

28. The method of claim 22 further comprising:

removing the sacrificial layer before forming the second layer.

29. The method of claim 22 wherein:

forming the second layer further comprises:

depositing the second layer;

disposing a photoresist layer over the second layer;

baking the photoresist layer over a range of temperatures;

exposing the photoresist layer to actinic radiation;

developing the photoresist layer;

etching the second layer; and

removing the photoresist layer after etching the second layer.

30. The method of claim 29 wherein:

baking the photoresist layer further comprises:

heating the photoresist layer over the range of temperatures during a first time period.

31. The method of claim 29 wherein:

forming the second layer further comprises:

avoiding exposing the photoresist layer to deep ultra violet light after developing the photoresist layer; and

avoiding exposing the photoresist layer to a baking process after developing the photoresist layer.

32. The method of claim 29 further comprising:

using the photoresist layer to directly protect portions of the second layer, the first layer, and the electrically insulative layer.

33. The method of claim 29 wherein:

baking the photoresist layer occurs only before exposing the photoresist layer.

Subt a6

34. The method of claim 20 further comprising:

designing the airbridge to have a design width,

wherein:

forming the first layer further comprises:

forming the first layer to have a first layer width greater than the design width; and

forming the second layer further comprises:

forming a portion of the second layer underneath edges of the first layer; and

keeping the second layer absent underneath a central portion of the first layer, the central portion of the first layer having the design width.